What is claimed is:

1. A digital image processor for use in a digital camera having an image capture unit arranged to output digital images and a memory for storing digital images, the digital image processor comprising:

a preprocessor comprising hardware for preprocessing digital images received from the image capture unit and storing the digital images in the memory; and

a postprocessor comprising hardware arranged to receive digital images and to postprocess the digital images into a viewable form.

2. A digital image processor as recited in claim 1 further comprising a system bus within the digital image processor, wherein the preprocessor, the postprocessor, and an interface for the memory are coupled to the system bus.

3. A digital image processor as recited in claim 2, wherein the postprocessor includes a color interpolator arranged to derive an unknown pixel color value associated with a first pixel based upon at least one known pixel color value associated with at least one other pixel using pixel color weight factors associated with an image sensor in the image capture unit.

4. A digital image processor as recited in claim 3, further including a color pattern setting buffer that is connected to the color interpolator and capable of storing image sensor data associated with the image sensor included in the image capture unit, the image sensor data being used to derive the associated pixel color weight factors.

5. A digital image processor as recited in claim 3, wherein the postprocessor further includes an RGB reconstructor that is connected to the color interpolator and capable of converting the digital image to an RGB format as needed.

6. A digital image processor as recited in claim 5, wherein the postprocessor further includes a digital image compressor connected to the color interpolator and the RGB reconstructor, the digital image compressor being capable of compressing digital images.

7. A digital image processor as recited in claim 6, wherein the color interpolator, the RGB reconstructor, and the compressor are each connected to the system bus.

8. A digital image processor as recited in claim 2, wherein the preprocessor includes a non-uniformity corrector capable of correcting non-uniformities included in the digital image received from the image capture unit.

9. A digital image processor as recited in claim 8, wherein the preprocessor further includes:

a programmable sampling filter that is connected to the non-uniformity corrector and capable of systematically selecting portions of the corrected digital image received from the non-uniformity corrector;

a modular transformer that is connected to the programmable sampling filter and capable of at least correcting aberrations in the sampled digital image received from the programmable sampling filter; and

a ditherer that is connected to the modular transformer and capable of at least correcting aliasing in the digital image received from the modular transformer.

10. A digital image processor as recited in claim 9, wherein the digital image processor further includes an authenticity stamping unit connected to the non-uniformity corrector and the system bus.

11. A digital image processor as recited in claim 10, wherein the authenticity stamping unit includes an authenticity stamper connected to a secure key buffer for storing a secure key, the authenticity stamper being capable of encryptically combining digital camera identification and the secure key with an associated non-uniformity corrected digital image.

12. A digital image processor as recited in claim 11, further comprising:

a memory interface controller connected to the system bus, the memory interface controller being capable of providing control signals suitable for controlling the storing of image data in and the retrieving image data from the memory;

a central processing unit (CPU) interface operatively connected to the system bus for managing communications between the digital image processor and a digital camera system CPU; and

system clock connected to the system bus, the system clock being capable of providing clock signals.

13. A digital image processor as recited in claim 12, wherein the non-uniformity corrector sends a first corrected digital image directly to the programmable sampling filter which, in turn, sends the sampled digital image to the system bus, the sampled digital image being capable of display on a viewer in a cineview mode, the cineview mode being capable of providing the digital camera with "through the lens viewing".

14. A digital image processor as recited in claim 13, wherein the non-uniformity corrector outputs an associated second corrected digital image to the system bus, the second digital image, in turn, being capable of storage in the memory in a capture mode.

15. A digital image processor as recited in claim 14, wherein the digital camera further includes an input/output (I/O) block suitable for coupling the microprocessor to external devices.

16. A digital image processor as recited in claim 2, wherein the postprocessor is arranged such that its operation does not interfere with the operation of the preprocessor or taking pictures using the digital camera.

17. A digital image processor as recited in claim 1, wherein:

the digital image processor is operable in a first mode in which data corresponding to preprocessed images from the preprocessor are directed to the memory, thereby bypassing the postprocessor; and

the digital image processor is operable in a second mode in which data corresponding to the preprocessed images from the preprocessor are directed to the postprocessor for postprocessing.

18. A digital camera comprising:

an image capture unit arranged to output digital images;

a digital image processor as recited in claim 1; and

memory for storing the digital images.